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EXAMINER	
ARENA, ANDREW OWENS	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 11/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,006	ANDERSON ET AL.	
	Examiner	Art Unit	
	Andrew O. Arena	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 24-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16,24,26,27,29 and 30* is/are rejected.

7)☒ Claim(s) *25 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al. (US 2004/0195628), hereinafter Wu, in view of McCaldin et al. (US 3,328,210), hereinafter McCaldin.

3. Regarding claim 1, Wu discloses (FIG. 5B) a field effect transistor (5,6; [0015] ln 1-2) (FET) comprising:

a source (FIGS 9A-10 ref 30 and 40; [0023] ln 8-10) region;

a drain (FIGS 9A-10 ref 30 and 40; [0023] ln 8-10) region;

a channel (FIGS 5B & 9A, area under gate 8 between source and drain is a channel) region disposed between the source and drain regions;

a bifurcated gate (8; [0018] ln 12-13; dictionary defines bifurcated as forked) region positioned over said channel region; and

a gate oxide layer (7; [0017] ln 5) adjacent to said gate region.

4. Further regarding claim 1, Wu differs from the claimed structure only in not disclosing "wherein said gate oxide layer comprises an alkali metal ion implanted." McCaldin is analogous art that teaches (Fig. 2) alkali metal ions implanted in the gate

oxide (25; col 2 ln 51-55). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the field effect transistor of Wu by implanting an alkali metal ion in the gate oxide, as taught by McCaldin; for at least the purpose of increasing channel conductance (col 4 ln 30-33).

5. Further regarding claim 1, the combined device of Wu and McCaldin discloses the alkali metal ion is implanted at a dosage calculated based on threshold voltage test data provided by a post silicide electrical test conducted on said FET, since any dosage amount is, or can be, "calculated based on threshold voltage test data provided by a post silicide electrical test conducted on said FET."

6. Regarding claim 2, Wu discloses (FIG. 5B) the transistor of claim 1, further comprising:

a substrate (1; [0015] ln 9);

an isolation layer (2; [0015] ln 10) positioned over said substrate;

and at least one fin structure (3 in transistors 5 & 6; [0016] ln 3) disposed between the source and drain regions (FIG. 9A: 30 & 40; [0023] ln 12-15);

wherein said source and drain regions are positioned over said isolation layer (FIG. 10 clearly shows source/drains 30 & 40 positioned over isolation 2).

7. Regarding claim 3, McCaldin teaches said alkali metal ion comprises cesium (col 1 ln 34-36, col 4 ln 30-33).

8. Regarding claim 4, Wu discloses (FIG. 5B) said transistor is one of a plurality of transistors comprised by a CMOS (complimentary metal oxide semiconductor) device (nMOS/pMOS 5/6; [0023] ln 12-15).

9. Regarding claim 5, Wu discloses (FIG. 5B) said plurality of transistors comprises a pFET (6) device ([0023] ln 12-15).

10. Regarding claim 6, the combined device of Wu and McCaldin differs from the claimed invention only in not expressly disclosing "an ion implantation level of said alkali metal ion is approximately 3×10^{18} cm^{-3}." McCaldin indicates the implantation level is adjustable: "...the effect of the electrical characteristics of the underlying semiconductor is a function of the bombardment time, beam current, oxide thickness and channel length... However, since none of these parameters are critical to device operability, selective variations may be made to obtain the desired characteristics" (col 4 ln 39-43, 46-49). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made that an ion implantation level of said alkali metal ion is approximately 3×10^{18} cm^{-3}; for at least the purpose of obtaining the desired channel conductance (col 4 ln 30-33).

11. Regarding claim 7, Wu discloses (FIG. 5B) said gate region comprises silicide (8; [0018] ln 2 & 12).

12. Regarding claim 8, the combined device of Wu and McCaldin teaches the claimed structure, therefore, it inherently teaches the claimed property of this structure: "said alkali metal ion adjusts nFET and pFET threshold voltages for the nFET and pFET devices by an amount required to match desired off-currents for said nFET and pFET devices."

13. Regarding claim 9, Wu discloses (FIG. 5B) a CMOS (complementary metal oxide semiconductor) device (nMOS/pMOS 5/6; [0023] ln 12-15) comprising:

raised source and drain regions (FIGS. 9A &10: 30 & 40; [0023] ln 12-15);

a channel region (FIGS 5B & 9A: area under gate 8 between source and drain is a channel) disposed between said source and drain regions;

a gate region (8; [0018] ln 12-13) positioned over said channel region;

a silicon layer (3; [0015] ln 7) dividing said gate region; and

a gate oxide layer (7; [0017] ln 5) adjacent to said gate region.

14. Further regarding claim 9, Wu differs from the claimed structure only in not disclosing "wherein said gate oxide layer comprises an alkali metal ion implanted." McCaldin is analogous art that teaches (Fig. 2) alkali metal ions implanted in the gate oxide (25; col 2 ln 51-55). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the field effect transistor of Wu by implanting an alkali metal ion in the gate oxide, as taught by McCaldin; for at least the purpose of increasing channel conductance (col 4 ln 30-33).

15. Further regarding claim 9 the combined device of Wu and McCaldin discloses the alkali metal ion is implanted at a dosage calculated based on threshold voltage test data provided by a post silicide electrical test conducted on said FET, since any dosage amount is, or can be, "calculated based on threshold voltage test data provided by a post silicide electrical test conducted on said FET."

16. Regarding claim 10, Wu discloses (FIG. 5B) the device of claim 9, further comprising:

a substrate (1; [0015] ln 9) ;

an isolation layer (2; [0015] ln 10) positioned over said substrate; and

at least one fin structure (3 in transistors 5 & 6; [0016] ln 3) disposed between the source and drain regions (FIG. 9A: 30 & 40; [0023] ln 12-15);

wherein said source/drain regions are positioned over said isolation layer (FIG. 10 clearly shows source/drains 30 & 40 positioned over isolation 2).

17. Regarding claim 11, McCaldin teaches said alkali metal ion comprises cesium (col 1 ln 34-36, col 4 ln 30-33).

18. Regarding claim 12, Wu discloses (FIG. 5B) a plurality of FET (field effect transistor) devices, wherein said plurality of FET devices comprises a pFET (6) device ([0023] ln 12-15).

19. Regarding claim 13, the combined device of Wu and McCaldin differs from the claimed invention only in not expressly disclosing "an ion implantation level of said alkali metal ion is approximately 3×10^{18} cm^{-3}." McCaldin indicates the implantation level is adjustable: "...the effect of the electrical characteristics of the underlying semiconductor is a function of the bombardment time, beam current, oxide thickness and channel length... However, since none of these parameters are critical to device operability, selective variations may be made to obtain the desired characteristics" (col 4 ln 39-43, 46-49). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made that an ion implantation level of said alkali metal ion is approximately 3×10^{18} cm^{-3}; for at least the purpose of obtaining the desired channel conductance (col 4 ln 30-33).

20. Regarding claim 14, Wu discloses (FIG. 5B) spacers (9; [0020] ln 1) separating said gate region from said source and drain regions.

21. Regarding claim 15, Wu discloses said gate region comprises silicide (8; [0018] ln 2 & 12).

22. Regarding claim 16, the combined device of Wu and McCaldin teaches the claimed structure, therefore, it inherently teaches the claimed property of this structure: "said alkali metal ion adjusts nFET and pFET threshold voltages for the nFET and pFET devices by an amount required to match desired off-currents for said nFET and pFET devices."

23. Regarding claim 24, Wu discloses (FIG. 5B) spacers (9; [0020] ln 1) separating said gate region from said source and drain regions.

24. Regarding claims 26 and 29, the combined device of Wu and McCaldin discloses said dosage of the alkali metal ion implantation is a function of a height of said fin structure divided by a thickness of said gate oxide multiplied by a calculated dosage level of said alkali metal ion implanted in a direction normal to said channel region, since any dosage amount is, or can be, "calculated as a function of a height of said fin structure divided by a thickness of said gate oxide multiplied by a calculated dosage level of said alkali metal ion implanted in a direction normal to said channel region."

25. Claims 27 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu and McCaldin as applied to claims 1 and 9 above, and further in view of Collaert et al. (US 2005/0020020) – hereinafter Collaert.

26. Regarding claims 27 and 30, Wu discloses (Fig 10) a conductor (13) on said source and drain regions. The combined device of Wu and McCaldin differs from the

claimed invention only in not disclosing the conductor is a silicide. Collaert is an analogous CMOS FinFET device that discloses (Fig 3b) a silicide (15; [0045]) on said source and drain regions. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Wu by forming a metal silicide on said source and drain, as taught by Collaert [0045]; at least because that is the common means of reducing contact resistance.

Allowable Subject Matter

27. Claims 25 and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

28. Applicant's arguments filed on 10/08/2005 have been fully considered but they are not persuasive. Applicant states "McCaldin introduces the ions into its gate oxide directly before the FET is complete. This is an important distinction between McCaldin and the Applicant's claimed invention, which provides implanting the ions after a silicide probe test occurs." Examiner does not concur with applicant's contention that this is an important distinction. The claimed invention is the same product disclosed in the prior art, the distinction argued by applicant lies only in the process of making the product:

> "Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

29. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). The field of endeavor is field effect transistors seeking, *inter alia*, to reduce leakage current; for both Wu ([0004] ln 15-20, [0005] ln 8-10) and McCaldin (col 2 ln 64-67). Furthermore, McCaldin indicates that the advantage of his inventive concept is not limited to his disclosed structure (col 4 ln 62-64). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the field effect transistor of Wu by implanting an alkali metal ion in the gate oxide, as taught by McCaldin; for at least the purpose of increasing channel conductance (col 4 ln 30-33).

30. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Conclusion

31. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is (571) 272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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